1

2

1

2

CLAIMS

What	is	claimed	is:
------	----	---------	-----

1	1. An apparatus, comprising:
2	a first memory cell coupled to a first bit line;
3	a second memory cell coupled to a second bit line;
4	an address decoder coupled to the first and second memory cells to
5	enable access to the first and second memory cells; and
6	a comparator circuit coupled to the first and second bit lines to compare
7	the voltage level on the first bit line with the voltage level on the second bit at a
8	time when data is output from the first memory cell on the first bit line and
9	from the second memory cell on the second bit line.

- 1 2. The apparatus of claim 1, wherein the address decoder decodes 2 part of a memory address.
 - 3. The apparatus of claim 1, wherein the first and second memory cells are dynamic RAM memory cells.
 - 4. The apparatus of claim 1, wherein the first and second memory cells are static RAM memory cells.
- 5. The apparatus of claim 1, wherein the comparator circuit is comprised of a single comparator with a first input coupled to the first bit line and a second input coupled to the second bit line.

1

2

1

l	6. The apparatus of claim 5, wherein the output of the comparator is
2	coupled to a latch to store an indication that the voltage level on the first bit line
3	differs substantially from the voltage level on the second bit line.

- 7. The apparatus of claim 6, wherein the time at which the latch is triggered is adjustable.
- 1 8. The apparatus of claim 6, wherein the latch is a sticky latch that is 2 triggered to latch an indication that the voltage level on the first bit line differs 3 substantially from the voltage level on the second bit line at any time that such 4 an indication takes place.
 - 9. The apparatus of claim 1, wherein the comparator circuit is comprised of:
- a subtracting circuit with a first input coupled to the first bit line and a second input coupled to the second bit line;
- a first comparator coupled to the output of the subtracting circuit; and a second comparator coupled to the output of the subtracting circuit.
 - 10. The apparatus of claim 9, wherein:
- the output of the first comparator is coupled to a first latch to store an
- indication that difference in voltage levels between the first bit line and the
- 4 second bit line has risen above a first reference voltage; and
- the output of the second comparator is coupled to a second latch to store
- an indication that the difference in voltage levels between the first bit line and
- the second bit line has dropped below a second reference voltage.

1

- 1 11. The apparatus of claim 10, wherein the first and second reference voltages are adjustable.
- 1 12. The apparatus of claim 10, wherein the time at which the first and 2 second latches are triggered is adjustable.
- 1 13. The apparatus of claim 10, wherein the first and second latches are
- 2 sticky latches such that the first latch will latch any indication that the
- differences in voltage level between the first and second bit lines has risen
- 4 above the first voltage reference and the second latch will latch any indication
- 5 that the differences in voltage level between the first and second bit lines has
- 6 dropped below the second reference voltage.
 - 14. A method, comprising:
- writing identical values to the first and second memory cells;
- 3 coupling a first memory cell to a first bit line;
- 4 coupling a second memory cell to a second bit line;
- 5 coupling the first and second bit lines to inputs of a comparator circuit;
- 6 reading the identical values from the first memory cell through the first
- 7 bit line and from the second memory cell through the second bit line;
- 8 comparing the voltage levels on the first and second bit lines.
- 1 15. The method of claim 14, further comprising latching an indication
- 2 from the comparator circuit that the voltage level of the first bit line differs
- 3 substantially from the voltage level of the second bit line.

- 1 16. The method of claim 14, further comprising setting the degree to 2 which the difference in voltage levels between the first bit line and the second
- 3 bit line is substantial.
- 1 17. A comparator circuit in a memory array comprising:
- a first input coupled to a first bit line that is coupled to a first memory
- 3 cell in the memory array;
- a second input coupled to a second bit line that is coupled to a second
- 5 memory cell in the memory array; and
- 6 an output coupled to a sticky latch.
- 18. The comparator circuit of claim 17, wherein the comparator circuit
- 2 is coupled to a multiplexer to disconnect the second bit line, and to connect a
- third bit line that is coupled the first memory cell in the memory array.